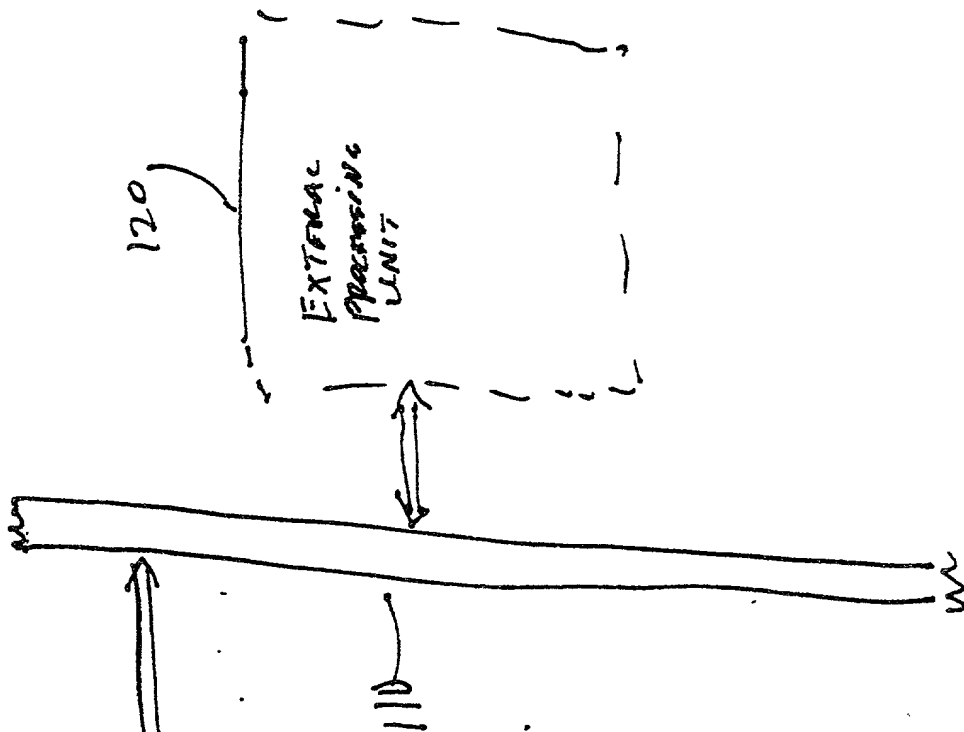
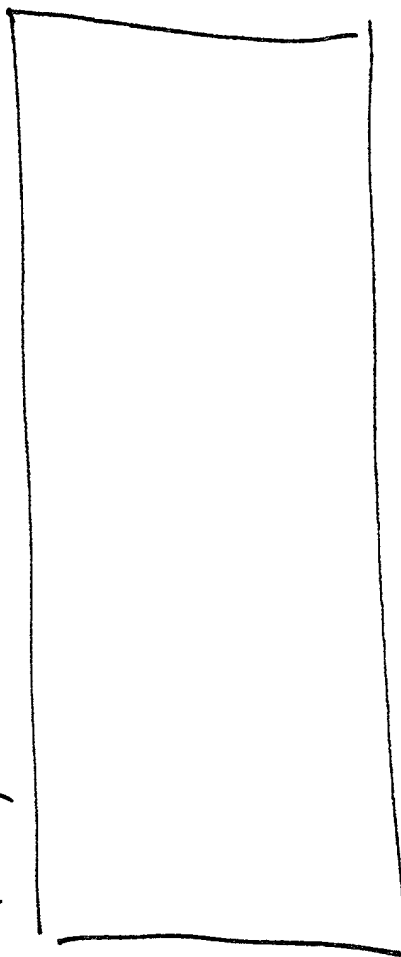
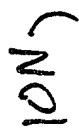
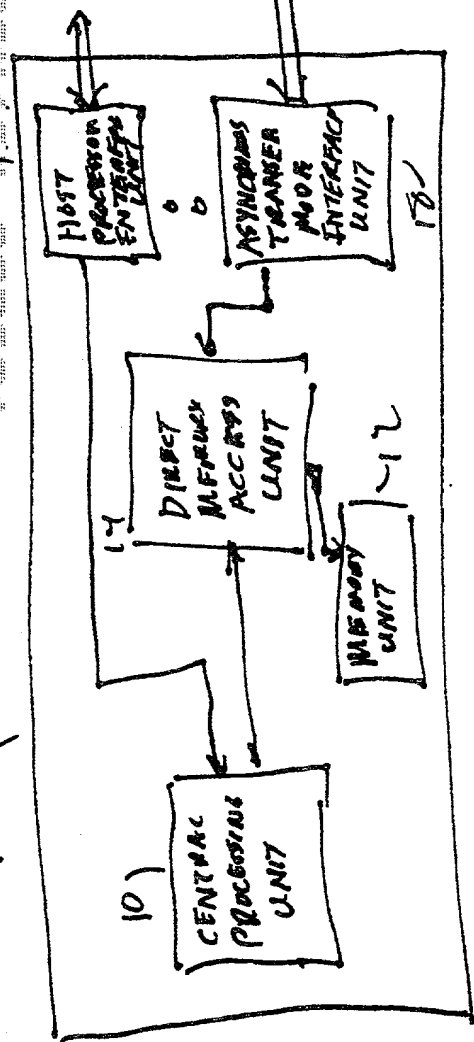
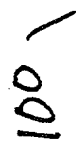


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15

1847

1827

147

DIRECT
MEMORY
ACCESS
UNIT

DATA [31:0]

ADDR [31:0]

WD-WR

EVENT

BUFFER
MEMORY
UNIT

DATA
[31:0]

CLAY

IND-RDY

PROCESSOR
(STATE
MACHINE)

UXCLK

UXADDR [24:0]

UXCLAY

UXENB

UXSOC

UXDATA
[15:0]

Fig. 2

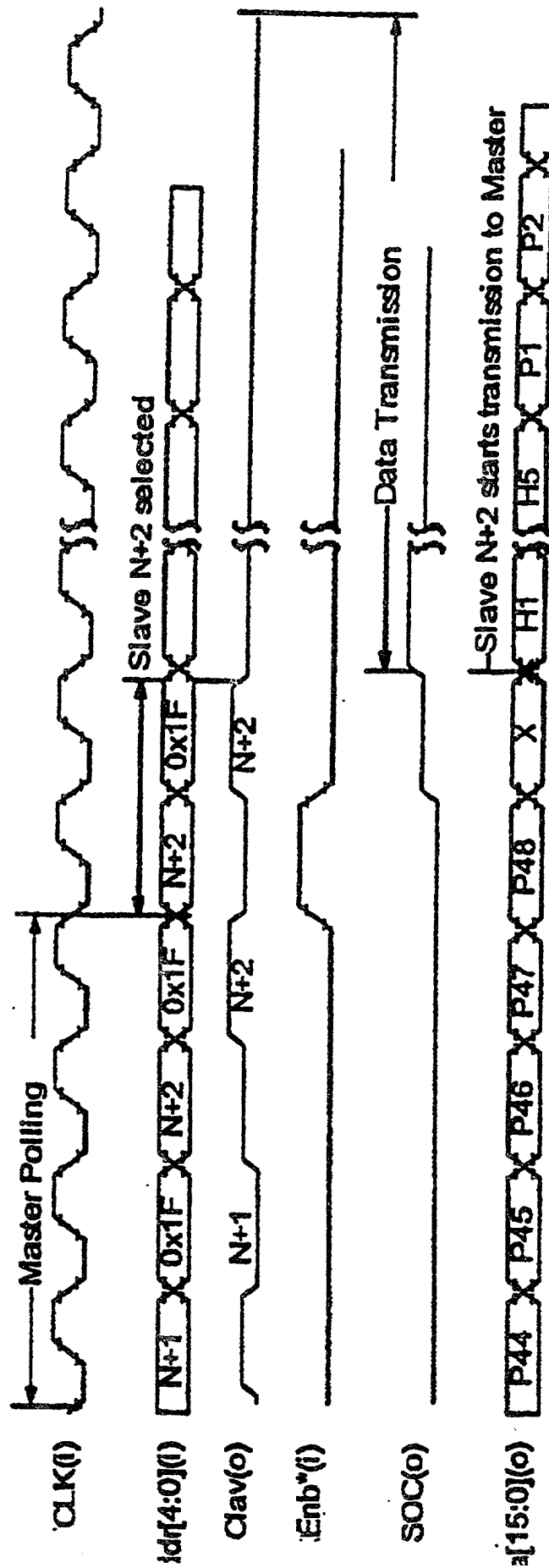


Fig. 3

147

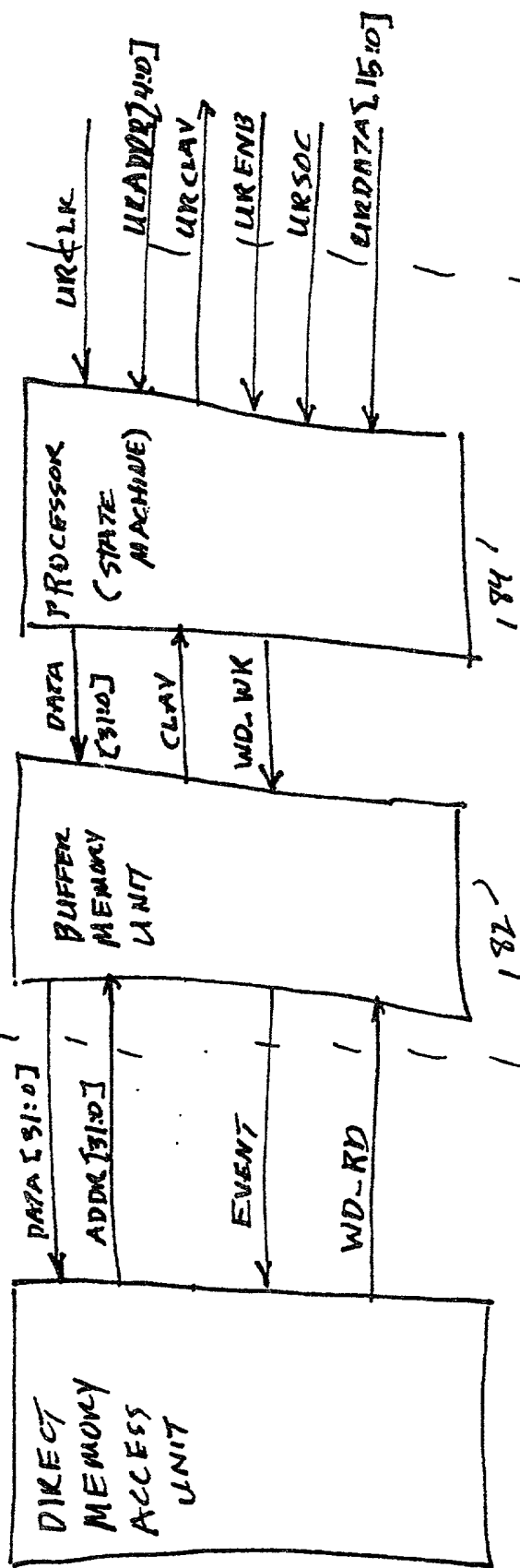


Fig. 4

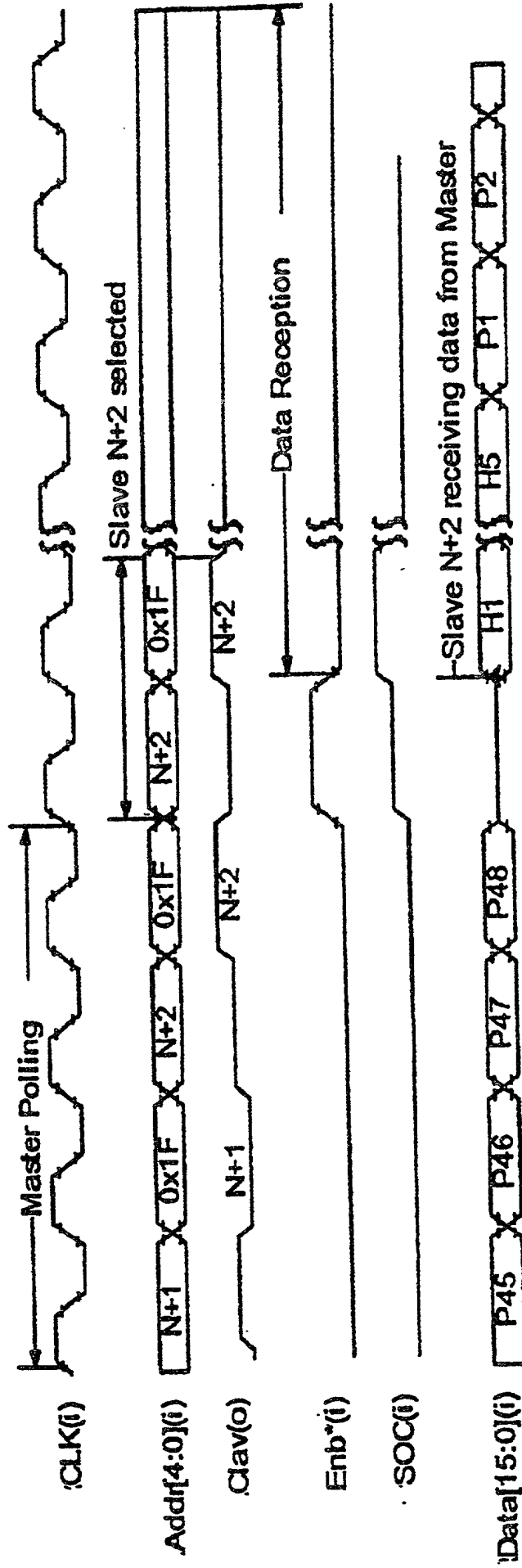


Fig. 5

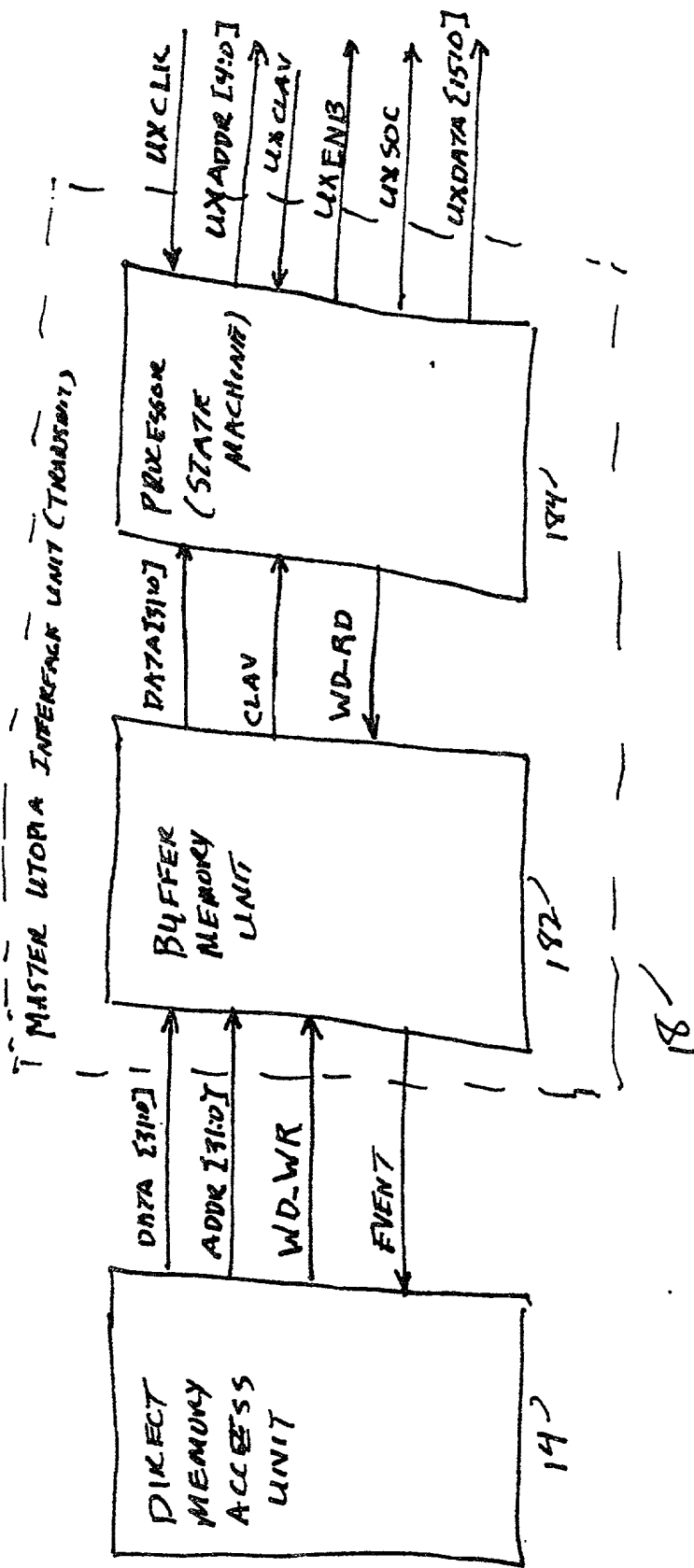


Fig. 6

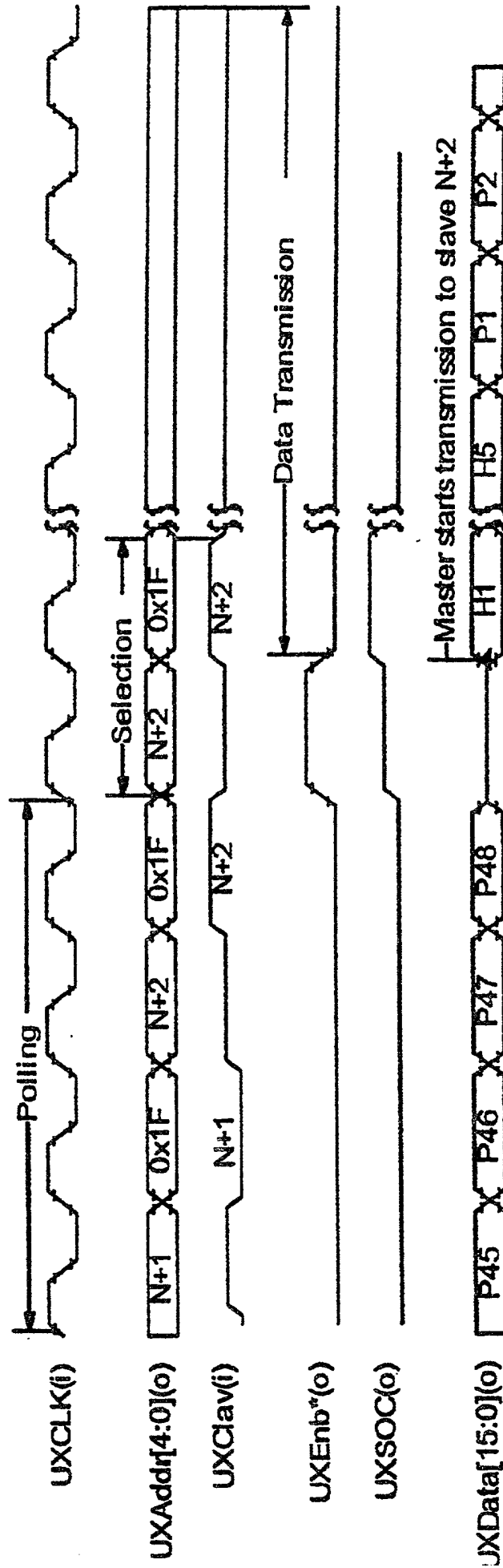


Fig. 17

TI-33533

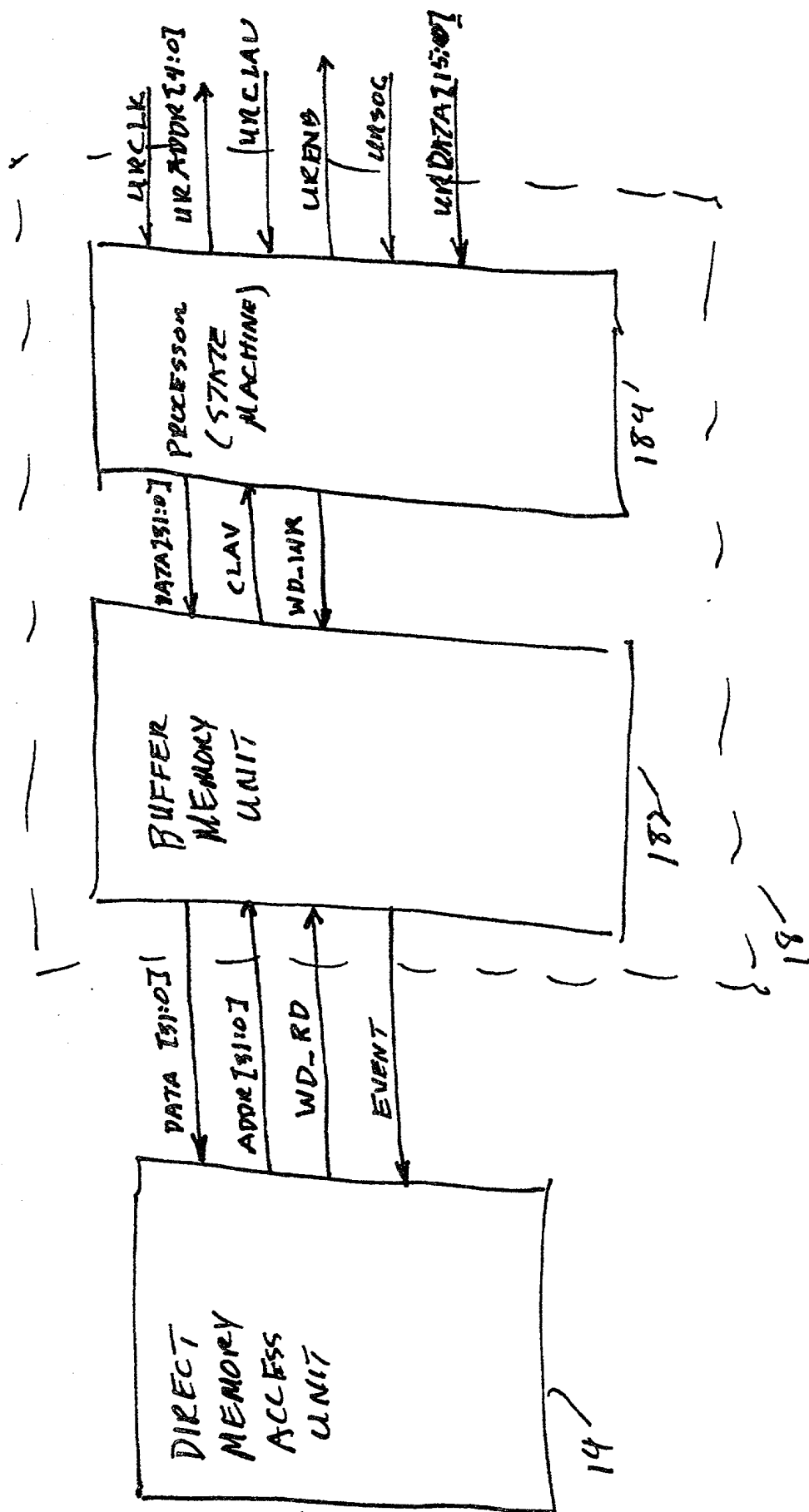


Fig. 8

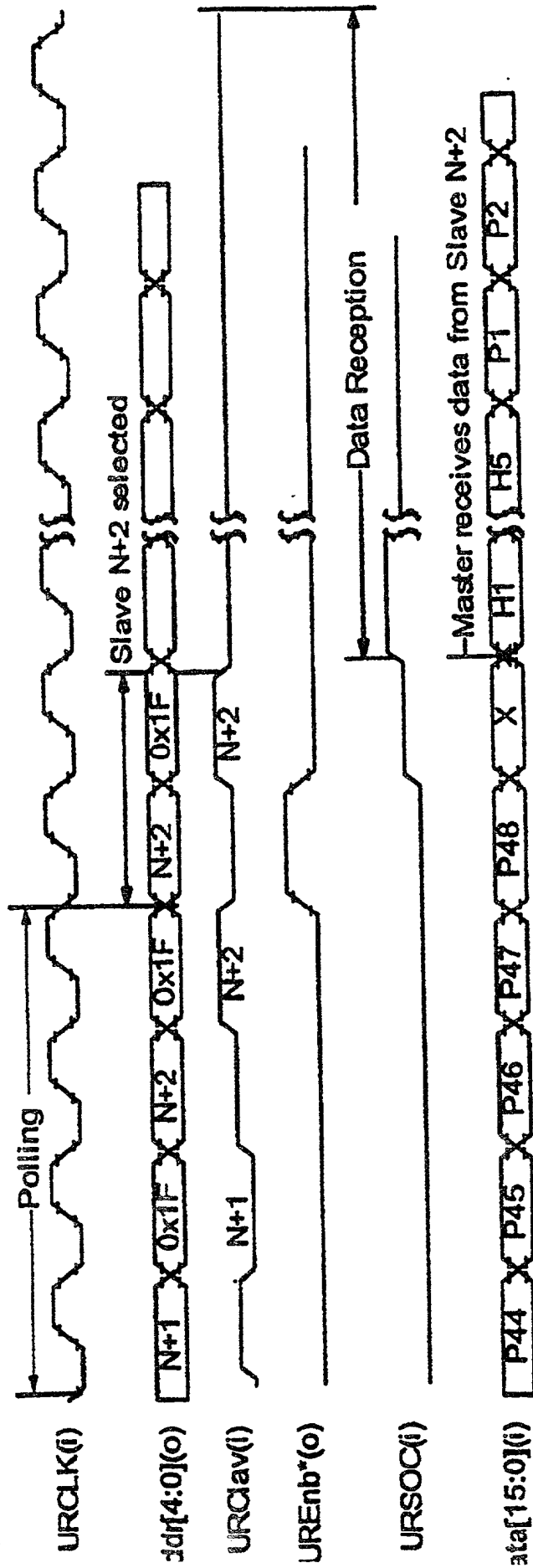
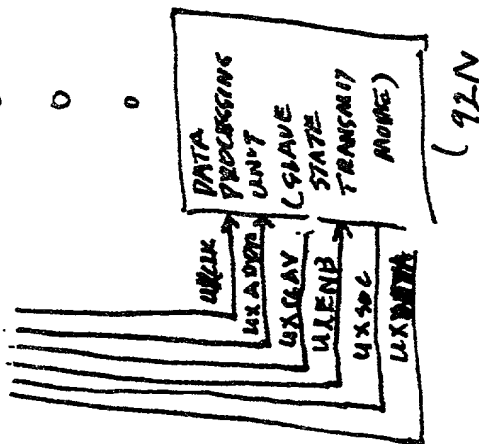
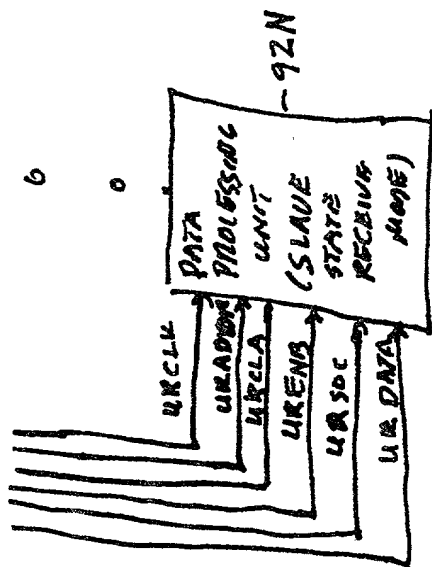
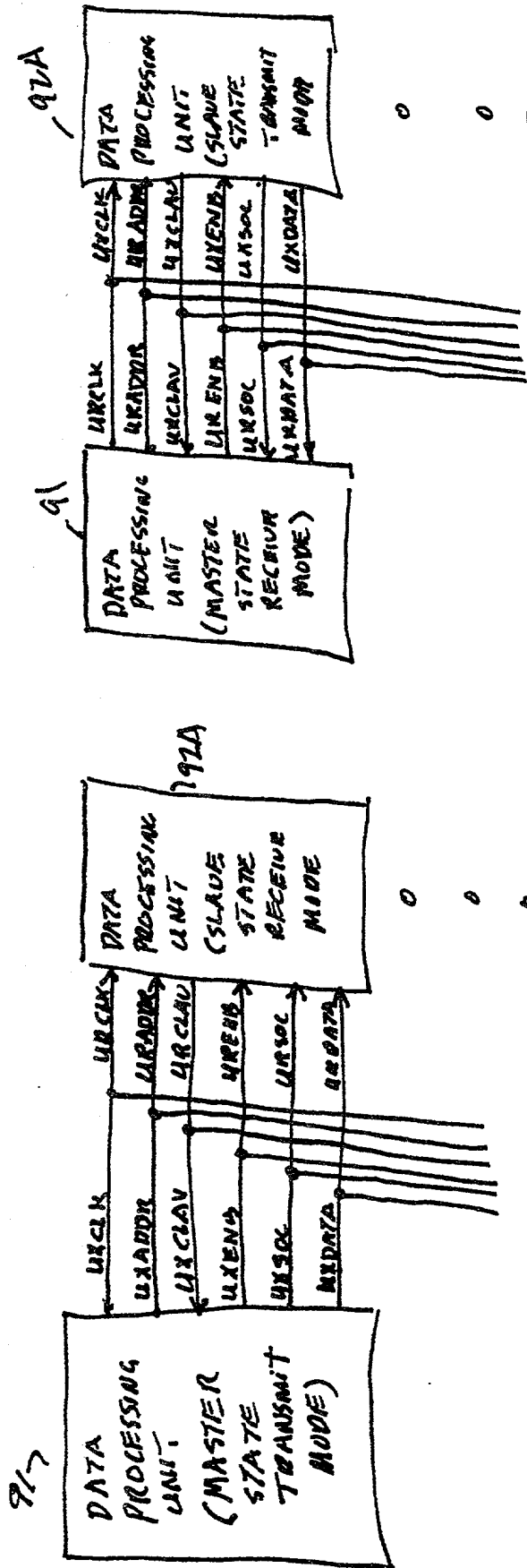


Fig. 9



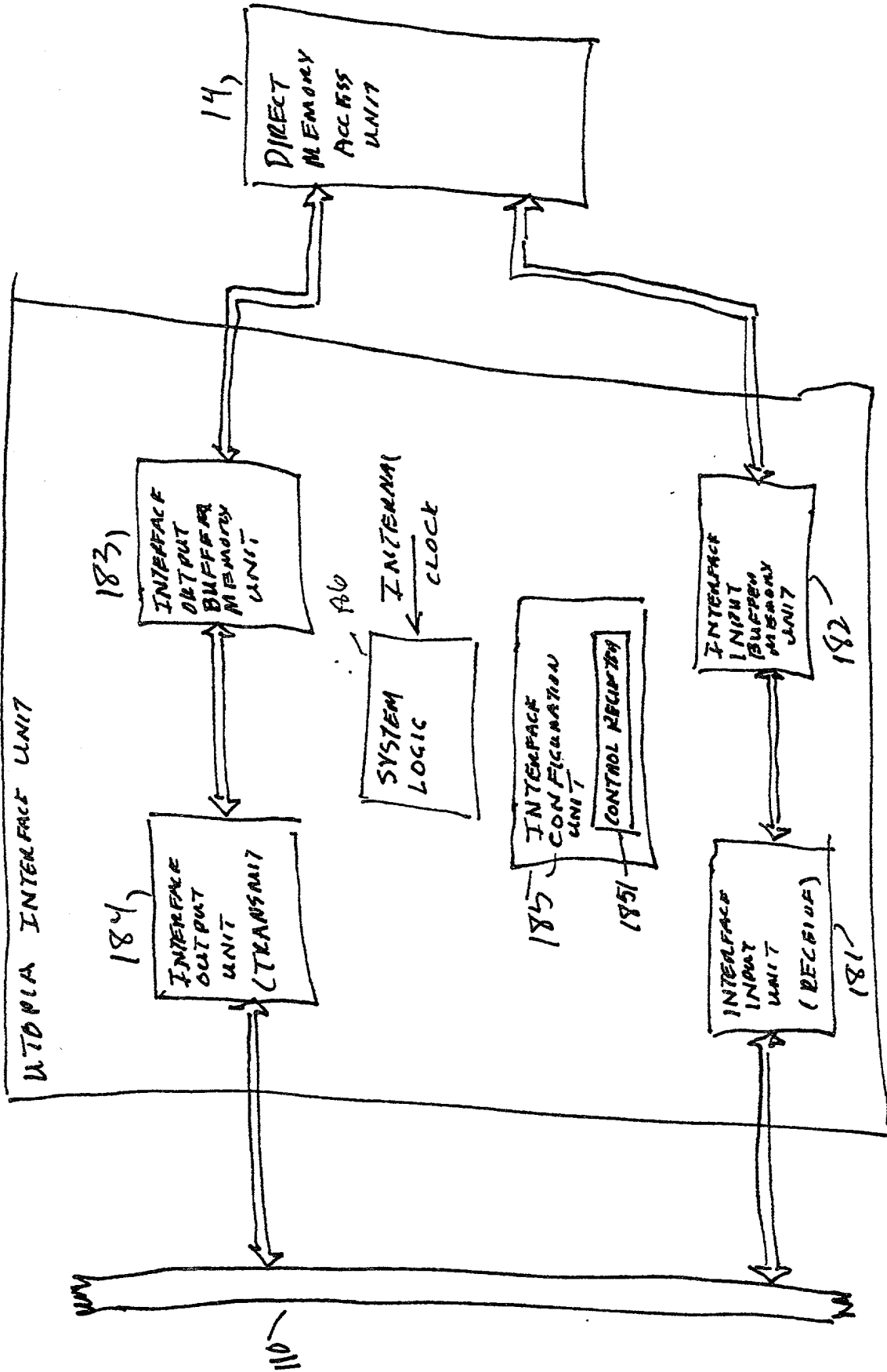


Fig. 11

31	END	30	Rsv	29	Rsv	28:24	SLID / SLEND	23:22	Rsv	21:18	XUDC	17	UXMSTR	16	UXEN
15	JLB	14	MPHY	13	U16M	12	UPM	11:10	Rsv	9:8	Rsv	7:6	ISV	5:2	RUDC
														1	0
														URMSTR	UREN

Fig. 12

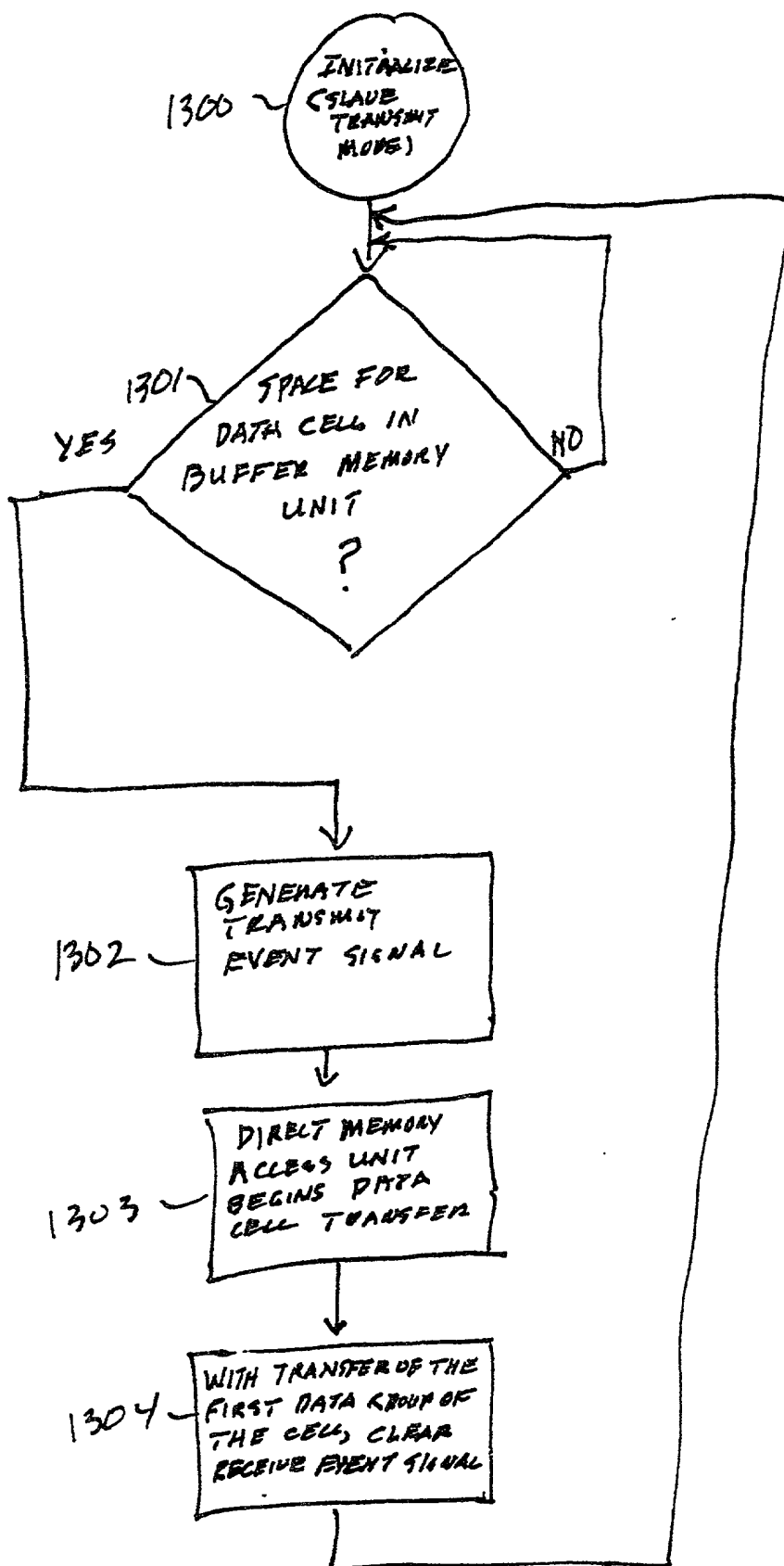


Fig. 13

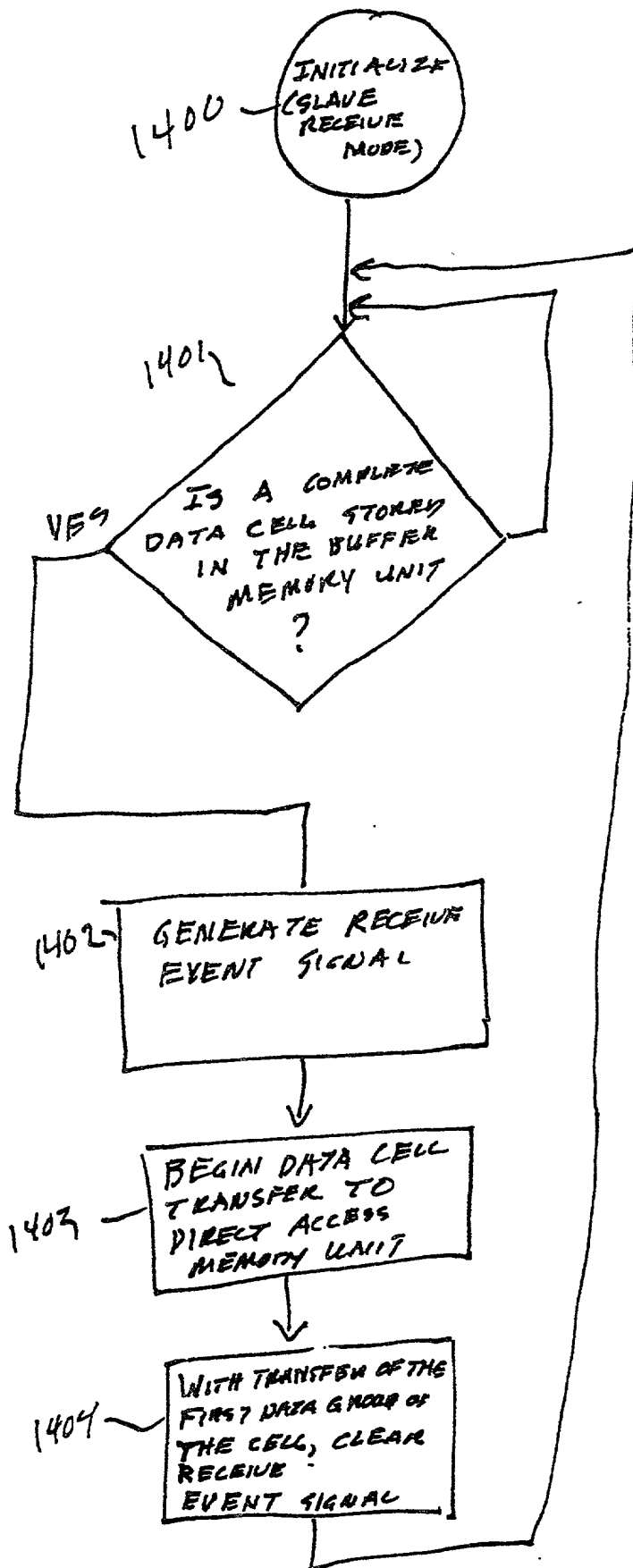


Fig. 14

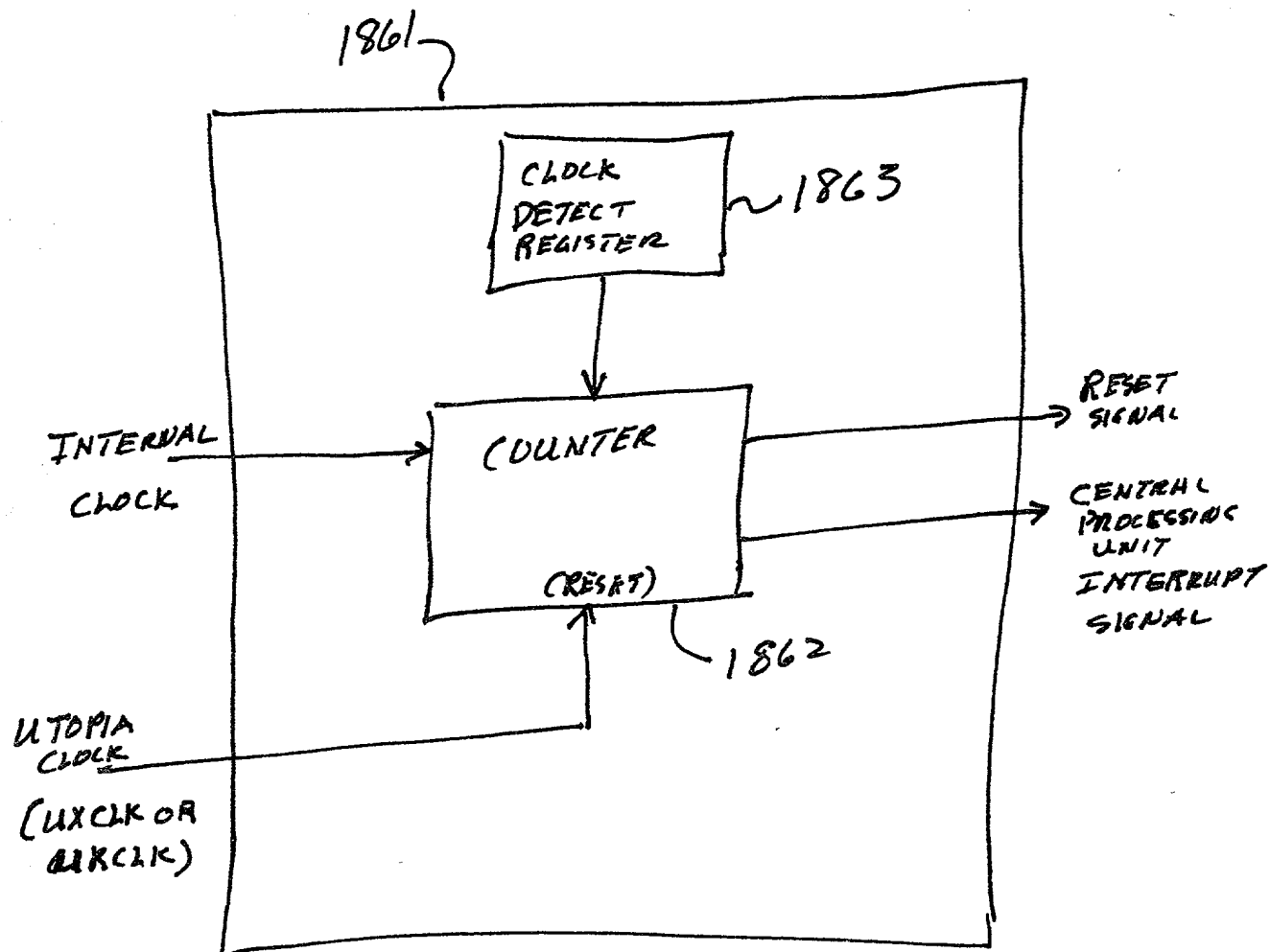


Fig. 15